



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|-----------------|-------------|----------------------|---------------------|------------------|
|-----------------|-------------|----------------------|---------------------|------------------|

09/781,128

02/09/2001

Patrick J. LaCour

MEGC116848

1693

26389

7590

05/20/2004

CHRISTENSEN, O'CONNOR, JOHNSON, KINDNESS, PLLC
1420 FIFTH AVENUE
SUITE 2800
SEATTLE, WA 98101-2347

EXAMINER

CHU, CHRIS C

ART UNIT

PAPER NUMBER

2815

DATE MAILED: 05/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application N .

09/781,128

Applicant(s)

LACOUR ET AL.

Examiner

Chris C. Chu

Art Unit

2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 27 February 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 15 - 19, 21, 23 - 27 and 35 - 49 is/are pending in the application.
- 4a) Of the above claim(s) 15 - 19, 21 and 23 - 27 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 35 - 49 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Response to Amendment

1. Applicant's amendment filed on February 27, 2004 has been received and entered in the case.

Claim Objections

2. Claims 35, 41, 46, 48 and 49 are objected to because of the following informalities:
In claim 35, line 8, the limitation "and/or" should be --and--.
In claim 41, line 9, the limitation "and/or" should be --and--.
In claim 46, line 9, the limitation "cells and" should be --cells,--.
In claim 48, line 8, the limitation "and/or" should be --and--.
In claim 49, line 3 from the bottom, the limitation "the one or more" should be --one or more--.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.
4. Claims 46, 47 and 49 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which

Art Unit: 2815

was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

In claims 46, 47 and 49, since the hierarchy of the input data file is preserved from start to the end of the process, the specification fails to disclose the step of "reducing the hierarchy of the input data file to include a number of selected cells and the one or more remainder cells".

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 35 – 49 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claims 35, 41, 46, 47, 48 and 49, the phrase "may" renders the claim indefinite because it is unclear whether the limitation(s) following the phrase are part of the claimed invention.

Regarding claims 38, 39, 43 and 44, the claims are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. See MPEP § 2172.01. The omitted structural cooperative relationships are: There is a structural functional problem between the limitation of "cells that are repeated in the layer of the integrated circuit" (e.g., claim 38), cells that maximize/minimize the area/time required to write modified/selected cells on the mask (e.g., claim 39). Applicant claims all cells except repeated

cells and cells that maximize and minimize area/time and the claims have not yet recited how repeated cells and cells that maximize/minimize area/time are related to the method or any of the steps of the method that describes the integrated circuit layer. Furthermore, the reference numbers "P14" in cell B (52), "P16" in cell C (54) and "P18" in cell T (50) are not repeated in the layer of the integrated circuit. However, the cells are selected and modified (see Figs. 5A – 5C).

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 35 – 49 are rejected under 35 U.S.C. 102(e) as being anticipated by Chang et al. '679.

Regarding claim 35, Chang et al. discloses in e.g., Fig. 1, Fig. 2, column 10, lines 47 – 67 and column 13, lines 15 – 35 a method of creating a file that describes a layer of an integrated circuit for use by a mask writing tool, comprising:

- receiving (220) a hierarchical input file (205) that defines a number of cells, each of which defines one or more polygons corresponding to patterns to be created on a mask, and may include references to other cells;
- selecting one or more cells (210) from the hierarchical input file;

- modifying the selected cells (260 in the output data 250) to include the polygons or portions thereof of non-selected cells and to compensate for interactions with other cells;
- creating one or more remainder cells (205 in the output data 250) to include polygons or portions thereof defined in the placements of non-selected cells that are not within the modified, selected cells; and
- creating a file (275) for use by a mask writing tool by eliminating the non-selected cells such that the description of the modified, selected cells and the one or more remainder cells with their placements describe the layer of the integrated circuit.

Regarding claim 36, Chang et al. discloses in e.g., Fig. 1, Fig. 2, column 10, lines 47 – 67 and column 13, lines 15 – 35 each cell having an extent, and the extents of at least some of the modified, selected cells to be written on the mask overlap.

Regarding claim 37, Chang et al. discloses in e.g., Fig. 1, Fig. 2, column 10, lines 47 – 67 and column 13, lines 15 – 35 the step of creating one or more remainder cells (205 in the output data 250) including to create a cell with polygons that prevent extraneous patterns from being created on a mask when the modified selected cells are written on the mask.

Regarding claim 38, Chang et al. discloses in e.g., Fig. 1, Fig. 2, column 10, lines 47 – 67 and column 13, lines 15 – 35 the selection of cells being limited to cells that are repeated in the layer of the integrated circuit.

Regarding claim 39, Chang et al. discloses in e.g., Fig. 1, Fig. 2, Fig. 5, column 10, lines 47 – 67 and column 13, lines 15 – 35 the selection of cells being limited to cells that maximize

the area of the mask written with the modified, selected cells and minimizes the time required to write the modified, selected cells on the mask.

Regarding claim 40, Chang et al. discloses in e.g., Fig. 1, Fig. 2, Fig. 5, column 10, lines 47 – 67 and column 13, lines 15 – 35 the selected cells being modified by determining if the mask writer is capable of transforming the orientation of modified, selected cell and if not, creating a copy of the modified, selected cell that the mask writer can print in a proper orientation.

Regarding claim 41, Chang et al. discloses in e.g., Fig. 1, Fig. 2, column 10, lines 47 – 67 and column 13, lines 15 – 35 a computer readable media including a number of instructions that when executed by a computer cause the computer to perform a method for creating a file that describes a layer of an integrated circuit for use by a mask writing tool by:

- receiving (220) a hierarchical input file (205) that defines a number of cells, each of which defines one or more polygons corresponding to patterns to be created on a mask, and may include references to other cells;
- selecting one or more cells (210) from the hierarchical input file;
- modifying the selected cells (260 in the output data 250) to include the polygons or portions thereof of non-selected cells and to compensate for interactions with other cells;
- creating one or more remainder cells (205 in the output data 250) to include polygons or portions thereof defined in the placements of non-selected cells that are not within the modified selected cells; and

- creating a file (275) for use by a mask writing tool by eliminating the non-selected cells such that the description of the modified, selected cells and the one or more remainder cells with their placements describe the layer of the integrated circuit.

Regarding claim 42, Chang et al. discloses in e.g., Fig. 1, Fig. 2, column 10, lines 47 – 67 and column 13, lines 15 – 35 the instructions further cause the computer to create one or more remainder cells by creating a cell with polygons that prevent extraneous patterns from being created on a mask when the modified, selected cells are written on the mask.

Regarding claim 43, Chang et al. discloses in e.g., Fig. 1, Fig. 2, column 10, lines 47 – 67 and column 13, lines 15 – 35 the instructions further cause the computer to limit the selection to cells that are repeated in the layer of the integrated circuit.

Regarding claim 44, Chang et al. discloses in e.g., Fig. 1, Fig. 2, Fig. 5, column 10, lines 47 – 67 and column 13, lines 15 – 35 the instructions further cause the computer to limit the selection of cells to cells that maximize the area of a mask written with the modified, selected cells and minimizes the time required to write the modified, selected cells on the mask.

Regarding claim 45, Chang et al. discloses in e.g., Fig. 1, Fig. 2, Fig. 5, column 10, lines 47 – 67 and column 13, lines 15 – 35 the instructions further cause the computer to modify the selected cells by determining if the mask writer is capable of transforming the orientation of a modified, selected cell and if not, creating a copy of the modified, selected cell that the mask writer can print in a proper orientation.

Regarding claim 46, Chang et al. discloses in e.g., Fig. 1, Fig. 2, column 10, lines 47 – 67 and column 13, lines 15 – 35 a method of preparing a file that describes a layer of an integrated circuit to be used by a mask writer to create one or more masks, comprising:

- receiving (220) a hierarchical input data file (205) that defines a number of cells, each of which defines one or more polygons corresponding to patterns to be created on a mask, a placement of where the cell is to be printed, and may include references to other cells;
- reducing (the step 210; column 13, lines 15 – 35) the hierarchy of the input data file (205) to include a number of selected cells (modified cells; e.g., F1) and the one or more remainder cells (not modified cell; e.g., F2 which uses a pointer to point to the correction data of F1); and
- creating the file (275) for use by the mask writer that describes the layer of the integrated circuit by including the selected cells, the one or more remainder cells and their placements.

Regarding claim 47, Chang et al. discloses in e.g., Fig. 1, Fig. 2, column 10, lines 47 – 67 and column 13, lines 15 – 35 a computer readable media including a number of instructions that when executed by a computer cause the computer to perform a method of preparing a file that describes a layer of an integrated circuit to be used by a mask writer to create one or more masks by:

- receiving (220) a hierarchical input data file (205) that defines a number of cells, each of which defines one or more polygons corresponding to patterns to be created on a mask, a placement of where the cell is to be printed, and may include references to other cells;
- reducing (the step 210; column 13, lines 15 – 35) the hierarchy of the input data file (205) to include a number of selected cells (modified cells; e.g., F1) and one or more

remainder cells (not modified cell; e.g., F2 which uses a pointer to point to the correction data of F1); and

- creating the file (275) for use by the mask writer that describes the layer of the integrated circuit by including selected cells, the one or more remainder cells and their placements describe the layer of the integrated circuit.

Regarding claim 48, Chang et al. discloses in e.g., Fig. 1, Fig. 2, column 10, lines 47 – 67 and column 13, lines 15 – 35 a file that describes a layer on an integrated circuit for use by a mask writer to create one or more masks, wherein the file is created by:

- receiving (220) a hierarchical input file (205) that defines a number of cells, each of which defines one or more polygons corresponding to patterns to be created on a mask, an indication of where the cells should be placed, and may include references to other cells;
- selecting one or more cells (210) from the hierarchical input file;
- modifying the selected cells (260) to include the polygons or portions thereof of non-selected cells and to compensate for interactions with other cells;
- creating one or more remainder cells (205 in the output data 250) to include polygons or portions thereof defined in the placements of non-selected cells that are not within the modified, selected cells; and
- creating a file (275) for use by a mask writing tool by eliminating the non-selected cells such that the description of the modified, selected cells and the one or more remainder cells with their placements describe the layer of the integrated circuit.

Regarding claim 49, Chang et al. discloses in e.g., Fig. 1, Fig. 2, column 10, lines 47 – 67 and column 13, lines 15 – 35 a file that describes a layer of an integrated circuit for use by a mask writer to create one or more masks that is created by:

- receiving (220) a hierarchical input data file (205) that defines a number of cells, each of which defines one or more polygons corresponding to patterns to create on a mask, an indication of where the cells should be placed, and may include references to other cells;
- reducing (the step 210; column 13, lines 15 – 35) the hierarchy of the input data file (205) to include a number of selected cells (modified cells; e.g., F1) and one or more remainder cells (not modified cell; e.g., F2 which uses a pointer to point to the correction data of F1); and
- creating the file (275) for use by the mask writer that describes the layer of the integrated circuit by including the selected cells and the one or more remainder cells and their placements.

Response to Arguments

9. Applicant's arguments with respect to newly presented claims 35 – 49 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Winder et al., Yamamoto et al. and Pasch et al. disclose the OPC correction method.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chris C. Chu whose telephone number is 571-272-1724. The examiner can normally be reached on 11:30 - 8:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 517-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

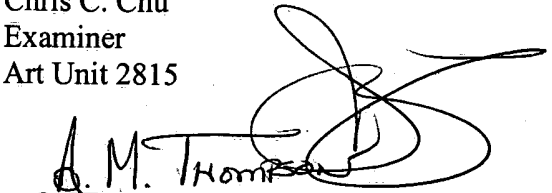
Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

Art Unit: 2815

system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chris C. Chu
Examiner
Art Unit 2815

c.c.
5/10/04 9:29:21 PM


D. M. Thompson
PRIMARY EXAMINER
TECHNOLOGY CENTER 2815